CLAIMS

What is claimed is:

1. A dielectric layer on a surface containing projections, comprising:

(a) a first conformal sublayer on said surface and projections, said first sublayer made of a first dielectric material characterized by plasma enchanced deposition;

(b) a second planarizing sublayer on said first sublayer, said second sublayer made of a second dielectric material characterized by plasma enchanced deposition.

2. The dielectric layer of claim 1, wherein:

(a) said first and said second dielectric materials are the same.

3. The dielectric layer of claim 1, wherein:

(a) said projections include insulated gates on a substrate; and

(b) said first and second dielectric materials are silicon oxides with at least one of said first and second materials including dopants.

4. A method of dielectric layer formation, comprising the steps of:

(a) plasma-enchanced depositing a first sublayer on a substrate with a plasma-to-substrate bias of less than a first threshold voltage; and

(b) plasma-enchanced depositing a second sublayer on a substrate with a plasma-to-substrate dc bias of greater than a second threshold voltage with said second threshold

voltage greater than said first threshold voltage.

5. The method of claim 4, wherein:

(a) said first threhsold voltage is less than about 150 volts; and

(b) said second threshold voltage is greater than about 300 volts.

6. The method of claim 4, wherein:

(a) said first and second sublayers are silicon oxides with at least one of said first and second sublayers including dopants.

7. A method of premetal dielectric fabrication for an integrated circuit, comprising the steps of:

(a) providing a substrate with insulated gate structures at a first surface; and

(b) plasma-enhanced depositing a dielectric layer over said gates and substrate with a plasma-to-substrate bias initially less than a first threshold voltage but increasing to greater than a second threshold voltage which exceeds said first threshold voltage;

(c) wherein said first threshold voltage is characterized by conformal deposition and said second threshold voltage is characterized by planarizing deposition.

8. The method of claim 7, wherein:

(a) said dielectric layer is made of silicon oxides.

9. The method of claim 8, wherein:

(a) said silicon oxides include dopants in at least a portion remote from said gate structures and substrate.

10. The method of claim 8, wherein:

(a) said silicon oxides include dopants in at least a portion adjacent said gate structures and substrate.